REMARKS

This responds to the Office Action mailed on June 13, 2007.

No claims are amended, canceled, or added; as a result, claims 1-25 remain pending in this application.

§102 Rejection of the Claims

Claims 1-25 were rejected under 35 USC § 102(e) as being anticipated by Moyes et al. (U.S. 7,065,688; hereinafter "Moyes").

First, Applicant does not admit that Moyes is prior art to the present application and reserves the right to swear behind Moyes at a later date.

Second, Applicant respectfully traverses the 35 U.S.C. § 102(e) rejection of claims 1-25 because Moyes fails to teach or suggest the inventive subject matter in the present application and current claims. For example, Moyes describes a memory initialization and testing method that performs initialization and testing in parallel at the processor level. In contrast, the subject matter of the present application and current claims performs memory initialization and testing in parallel at the memory module level, which is finer grain and allows parallel initialization and testing at a greater level.

Moyes in the paragraph beginning at line 47 of col. 5 describes that the memory initialization process is triggered by a Boot Strap Processor (BSP) which may send a start message to or set a start bit of each or all processing nodes. In the following paragraph, beginning at line 66 of col. 5, each processing node then performs initialization and testing for a portion of memory. Each processing node can then execute a routine that tests and initializes memory. Applicant respectfully submits that memory initialization and testing is performed at the processor level by a processor. Applicant is unable to locate any teaching or suggestion of performing memory initialization or testing at a lower level than at the processor level.

In contrast, the present application, as is illustrated in FIG. 1 and described in the paragraph beginning at line 12 of page 4, some embodiments of the inventive subject matter includes at least one processor 102, at least one memory controller 104, and main memory 106 which includes at least one bank 110 of memory modules 112, 114, 116. In some such

embodiments, the memory controller 104 receives initialization and/or memory test commences from the processor. Page 5, lines 22-23. The memory controller 104 passes those commands to memory modules 112, 114, 116. Page 5, lines 22-24. Such commands, as described in the present application in the paragraph beginning at line 15 of page 10 may command a memory module 300 to perform an initialization or test procedure on some or all of its associated memory. Thus, as described, memory initialization is performed at the memory module level and not at the processor level as in Moyes.

Applicant respectfully submits that the pending claims are directed to methods that perform the memory testing and/or initialization at the memory module level. For example, with *emphasis* added, the independent claims provide:

- **Claim 1:** the first memory access procedure causes *a memory module to perform* multiple accesses of first memory locations associated with the memory module….
- **Claim 5:** performing an initialization procedure, in response to the initialization command, during which *a memory module initializes* one or more memory storage units by generating and sending data packets with initialization data to the one or more memory storage units.
- **Claim 8:** performing a testing procedure, in response to the test command, during which *a memory module tests* one or more memory storage units by reading data within memory locations of the one or more memory storage units, and comparing the data with expected data.
- **Claim 12:** *a first memory module* performing a first memory access procedure … and *at least one additional memory module* performing a second memory access procedure….
- **Claim 16:** *a first memory module* performing a first initialization procedure of first memory locations associated with the first memory module; and *at least one additional memory module* performing at least one additional initialization procedure of second memory locations associated with the at least one additional memory module….
- **Claim 21:** generating and sending multiple memory initialization commands to *multiple memory modules* of a memory subsystem; the *multiple memory modules* receiving the multiple memory initialization commands; and selected ones of the *multiple memory modules* performing an initialization procedure in parallel, in response to receiving an initialization command.

Thus, although Moyes may be directed to parallelizing memory initialization and testing, Moyes parallelizes these tasks at the processor level which is discussed in the Background section of the present application. Applicant respectfully submits that the present claims are

novel over Moyes because the claims are directed to memory initialization and/or testing at a finer granularity of the memory modules.

Applicant respectfully requests consideration of the above distinctions between the present claims and Moyes and allowance of claims 1-25.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, James Hallenbeck ((612) 373-6938), or Applicant's below-named representative ((612) 349-9592) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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